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(54) Active surge rejection circuit.

(57) The ACTIVE SURGE REJECTION CIRCUIT uses a FET connected in one of the TIP and RING leads to open and close the lead. A JK flip-flop is connected to a voltage sensing circuit which senses voltage surges and clocks the flip-flop early in the voltage rise. This activates a first circuit to ground the FET gate and hold the FET open. Meanwhile, a second circuit comprising an RC circuit charges a capacitor which maintains the FET in its OFF condition for a period of time longer than the surge, i.e., about 1 m sec, and then clears the JK flip-flop after the capacitor has discharged a predetermined amount.

The combination of this invention and a transformerless DAA with pulse transformer digital isolation at the digital interface between the IA and the DSP synergistically provides both common and uncommon mode protection.

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BACKGROUND OF THE INVENTION

This application is related to simultaneously filed U.S. application entitled MODEM WITH DIGITAL ISOLATION by the same inventors, assigned to a common assignee.

Field of the Invention

The invention disengages electronic devices, including modems, from the power source and/or telephone line system when sensing high level, fast rising surges.

Prior Art

In the prior art the Data Access Arrangement (DAA), which interfaces between the telephone lines and the modem, employs an isolation transformer which is too large and heavy for the new "credit card" minimal size modem cards.

Just as data speeds are growing, modem size is decreasing. Modems are becoming an integral part of all LapTop/PalmTop computers. Because these computers are small, size and weight are at a premium. With the growing data rates, minimum distortion is a must. Distortion is the limiting factor for high speed modems.

While the DAA isolation transformer protects the electronic circuits, it also introduces distortion, consumes real estate and is the heaviest part of the modem section. In the case of portable computers, minimum weight is a priority requirement.

Some modems have eliminated the DAA isolation transformer by using analog optical isolation. However, distortion, cost and complexity remain the real problems.

Modems are very cost contemplative and the circuitry must not only be small but also the basic design must be compatible or adaptable to the current integrated circuit technology.

By eliminating the transformer and the distortion that comes with it, an increase in the data rate capabilities of the modem is realized. Size, weight and cost are also reduced significantly.

Although significant strides in improving performance and reducing the size of modems has been made, the DAA interface circuitry has remained relatively unchanged. In fact, on some of the lap top designs, the DAA occupies almost as much room as the remainder of the modem circuitry.

So far, designers have been able to stay within the packaging constraints by squeezing the parts closer together. However, designers are quickly reaching limits as they are now experiencing problems in meeting the UL and Part 68 high voltage breakdown test. In addition, the physical size of the DAA components prevents the installation of a modem in the new pocket computers.

One of the largest components in the DAA is the transformer. Functionally the transformer satisfies two design requirements.

First it provides the necessary high voltage isolation between the telephone network and the user. In the United States, this is specified by FCC part 68 which requires 1500 volts. In other countries this isolation may be up to 3750 volts.

Second it provides the balance interface circuit necessary to meet Part 68, as well as providing good common mode rejection of the noise signals normally on the telco lines.

To support both of these requirements and still maintain a very low distortion level results in a relatively large transformer. For example, the new high performance modems, like v.32, require distortion levels of -70dBm or lower. To achieve these levels require special magnetic material and large physical size.

Based on these problems, it is clear that there needs to be an alternate to the isolation transformer.

Experience indicates that when one attempts to add isolation circuitry in the analog circuit path, there will always be the problem of adding distortion.

SUMMARY OF THE INVENTION

The invention eliminates surge problems when the large isolation transformer is removed.

The modem must pass a metallic voltage surge test which is a pulse of 800 volts applied between the TIP and RING of the modem. While the modem is at the ON-HOOK state, there is no problem because the seizure relay is off (open), and thus, prevents the surge from getting into the electronic circuits. This 800 volt surge is also applied while the modem is in the OFF-HOOK state, at which time the line switch is closed and the 800 volt can cause an irreversible damage to our electronic circuits.

A FET is connected in one of the TIP and RING leads to open and close the lead. A JK flip-flop is connected to a voltage sensing circuit which senses voltage surges and clocks the flip-flop early in the voltage rise. This activates a first circuit to ground the FET gate and hold the FET open. Meanwhile an RC circuit charges a capacitor which maintains the FET in its OFF condition for a period of time longer than the surge, i.e., about 1 m sec, and then clears the JK flip-flop after the capacitor has discharged a predetermined amount.

A synergistic result is obtained if the above invention is combined with a transformerless DAA circuit which uses pulse transformers and multiplexers/demultiplexers or optical or other isola-

tion at the digital interface (rather than in the analog DAA) between the Integrated Analog and the Digital Signal Processor for isolation, resulting in minimal analog distortion, and higher data rates because both common mode and uncommon mode protection is obtained. The elimination of the heavy conventional isolation transformer is particularly helpful in cards for LapTop/PalmTop computers.

The present invention can provide surge protection/rejection as a stand alone circuit. In other words, while it complements the DIGITAL ISOLATION, it can serve other applications just as well.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a prior art modem;
FIG. 2 is a block diagram of the transformerless DAA;
FIG. 3 shows the surge detector and a line FET;
FIG. 4 shows a typical square wave;
FIG. 4A shows the wave differentiated to save power;
FIG. 5 shows coils for a pulse transformer in lieu of the conventional isolation transformer;
FIG. 5A is a view in cross section of a pulse transformer:
FIG. 6 shows a prior art surge protection circuit when the isolation transformer is present;
FIG. 7 shows the surge protection circuit of this invention in the absence of an isolation transformer; and,
FIG. 8 is a circuit diagram of a transformerless DAA circuit with surge protection.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Currently, the Rockwell modem Integrated Analog (IA) device 11 (FIG. 1) and the Digital Signal Processor 13 (DSP) are connected by 15 individual wires 15, with the micro processor 14 being connected to DSP 13 by two wires 16.. All Data Access Arrangement (DAA) devices 17 (FIG. 2) require a high voltage isolation between the telephone lines 19,21 and a modem. Usually transformer 21 (in the DAA section) provides this isolation.

FIGs. 2, 4, 4A, 5 and 5A detail the cross-referenced invention which eliminates the conventional isolation transformer from the DAA and provides a synergistic combination with the present invention, which is best seen in FIGs. 7 and 8.

In FIG. 2, the isolation transformer 21 has been eliminated and, instead, tiny pulsed transformers 25,27 are used between the IA device 11' and the DSP 13'. The received integrated analog signal is digitized, and then multiplexed in box 29 and demultiplexed in box 31, whereas the transmitted signal is multiplexed in Box 31A and demultiplexed in box 29A, thus avoiding the 15 wire interconnection and all analog distortion.

Thus, it may be seen that the parallel signals on these leads (15) are combined into two serial data streams, one input and one output. The data is encoded in a time division multiplex, self clocking arrangement. All serial encoding and decoding is incorporated into the Integrated Analog and Digital Signal Processing devices 11' and 13', so that the isolation circuitry may consist only of two pulse transformers 25, 27 or two opto couplers (not shown).

Also, pulsed signals save power. It is only necessary to pass short spikes 35,37 (FIG. 4A), representing up and down transitions of original wave 39, rather than to pass the full wave 39 (FIG. 4). Common mode rejection, as well as, high voltage isolation are attained by the pulse transformers.

FIGs. 5 and 7 show the construction of the pulse transformers 25 and 27 on conventional glass pc board 41 of, e.g., .062" thick. Center holes 36,38 in the board, receive the legs 42,43 and 44,45 of U-bars 40,46 to form the "gaps" where they abut. The coils 37,39 surrounding the respective legs comprise only a few turns of metal, laid down on the board 41, and etched away to leave the coils, which may have diameters of about 1/8 inch. The U-bars are about 1/2 inch in length. The other pulse transformer 27 is spaced away from transformer 25 as far as practical, and the components are the same, bearing the primes of the same numbers. The best magnetic materials are employed for the magnetic path, such as ferrite, and the small dimensions easily fit space minimums.

The frequency of operation is in the megacycle range, and the power losses are extremely low because the pulse technique requires much less power than handling the entire wave. The pulse technique also handles common mode distortion problems.

In lieu of the preferred pulse transformers at the digital interface, other types of isolation may be used. Two opto couplers are also effective on two serial data streams, i.e. one input and one output, but the pulse transformer isolation uses less power.

For non-common mode, e.g., lightning caused surges, i.e., in above ground telephone systems, the block diagrams of FIGs. 3 and 7 show surge rejection circuits for use in DAA device 17 of FIG. 2. In FIG. 3, TIP line 51 includes FET 52 (or a fast acting transistor) to open this line. DETECTOR 53 between TIP lead 51 and RING lead 54, senses the surge and very quickly opens FET 52.

FIG. 6 shows PRIOR ART type surge protection for modems, e.g., 57 coupled to telephone lines 58,59. The conventional isolation transformer 60 is shown connected between the telephone lines 58,59 and the modem 57. MOV 61 (metal oxide varistor) is shown connected across the lines to act as a surge absorber. RING DETECTOR 62 is provided to indicate to modem 57 that a ring has appeared and the DSP 13, via IA11, operates LINE SEIZURE RELAY 63.

FIG. 7 shows a preferred surge protection circuit of this invention in the absence of isolation transformer 60. The details of this SURGE REJECTION and LINE SEIZURE SWITCH 65 are set forth in FIG. 8.

In FIG. 8, the ON and OFF Hook lead is shown at 101, supplying +5 volts in OFF HOOK, and the D.C. power lead 103 receives +5 volts above ground 105 when the MODEM is on. FET 107 (BUZ 78) serves to open and close TIP lead in the signalling circuit for unexpected surges.

Capacitor 110 in parallel lead 111, including series resistor 112 across TIP lead 109 and RING lead 113, is a .33 μf, 250 volt capacitor and resistor 112 is 10,000 ohms. The pair comprise a dummy load for the RING signal.

Next, a full wave bridge rectifier comprises the four 1N4006 diodes 115, 117, 119 and 121 to insure positive voltage on the drain 123 of FET 107, source 125 being grounded at 105 over lead 127.

The circuit of FIG. 8 must provide protection under a variety of circumstances:

1) The modem's power is OFF at 103.

At this time the FET 107 (Q4) is already in the OFF state. While in the OFF state, the FET will block high voltage from going through. When the fast rising surge arrives, it attempts to charge the FET gate 129 through the internal capacitance of the FET 107. Normally, this will cause the FET to turn ON. However, diode (1N1148) D12 131 keeps the FET 107 OFF by clamping the gate 129 to ground 105 via the 5v power supply, thus, preventing any charge build-up on the gate 129.

2) The modem's power is ON at 103 and it's ON-Hook at 101.

This case is similar to the previous one in the sense that the FET 107 is still OFF and no DC current is running through it. The FET is OFF because the ON-Hook signal coming through lead 101 keeps the gate 129 at ground level 105. At this time, the JK flip-flop 133 (U2) (74HC112) is powered from lead 103 and can assist in keeping the FET 107 OFF. When the surge arrives it will pass through C4, shown at 135 (100pf) and becomes a clock to the JK flip-flop 133. Resistor R6, shown at 161, has 47,000 ohms and resistor R4, shown at 162 has 10,000 ohms. This 5:1 ratio determines the extent of the surge voltage necessary to clock JK flip-flop 133 over lead 137, and it can be made adjustable, if desired. As a result the Q output of the JK 133 will go up and turn Q2 140 (2H1222) ON over leads 138 and 127, and 131. Q2 140 will hold the gate 129 of Q4 140 clamped to ground level, which results in keeping the FET 107 at the OFF state.

3) The modem's power is ON at 103 and it's OFF-Hook at 101.

This time around, the FET 107 is conducting line current because its gate receives 5v from the lead 101. The surge will, again, go through C4 135 and clock the JK 133. The Q output of JK will go up and cause Q2 140 to turn ON. Q2 140 will turn the FET 107 OFF as soon as possible before the voltage builds up.

4) The modem's power is ON at 103 and it's OFF-Hook at 101 but no current flows through TIP and RING.

This time the circuit performs the same way as in the last case. This situation is not likely to happen during normal use of the modem, but FCC labs do test the modem powered ON with no TIP and RING current.

In support of the above activities, Q12 142 (2N4403) turns ON any time the JK flip-flop 133 gets clocked and will turn Q14 144 (MJD 47) ON very fast. This action discharges the stray capacitance and the FET's 107 capacitance, preventing a voltage build-up. R10 145 (47K) and C6 147 (.01μf) hold the Q output of the JK flip-flop 133 at a high level which keeps the FET 107 OFF for about 1mSec. This way the FET 107 is turned OFF for a period longer than the expected duration of the surge. In case the surge persists beyond (1MS) the R7 & R5 C5 combination was designed to keep the JK at the clocked state which in turn keeps in turn keeps Q4 107 off.

It should be noted that, for AC purposes, ground 105 is connected to +5 volt lead 103, so a high potential spike or surge across TIP-RING causes the negative side of the pulse to pass via any or several paths in the electronic inductor box 150 up to ground 105 and to lead 103. Thus, the pulse is across the 5:1 voltage divider, R4 162, R6 161.

Also, when FET 107 is going from ON to OFF, there is still some energy passed through it, and voltage builds up across Q14, 144. After the clock, transistor Q12 142 turns on hard by Q bar, Q going up and Q14 144 is then turned on hard, absorbing the energy.

The surge protective circuit can work in any circuit or modem to protect, e.g., consumer products from non-common mode surges. Thus, the

combination of the transformerless DAA with digital pulse transformers and the surge protection circuit precludes both uncommon mode and common mode problems.

The invention may be summarized as providing a modem surge protection circuit, comprising in combination:
TIP and RING leads for communication between the telephone lines and the modem;
a FET means connected to open and close one of said leads; and
an ON/OFF HOOK circuit for supplying operating voltage to said FET means when in the OFF HOOK mode.

Preferred embodiments of the invention are disclosed in the claims and also the dependent claims, which should be read as depending not only on the specified claims, but on any other claim and combination thereof. The same is true for the following summary of the invention:

The invention may be summarized as follows:

1. A modem surge protection circuit, comprising in combination:
TIP and RING leads for communication between the telephone lines and the modem;
a FET connected to open and close one of said leads;
an ON/OFF HOOK circuit for supplying operating voltage to said FET when in the OFF HOOK mode;
a modem power source for dc voltage which is positive relative to ground;
a first circuit and a second circuit;
a flip-flop circuit for activating said first circuit in one condition and said second circuit in its other condition;
sensing means connected across said leads for activating said flip-flop circuit to said one condition upon sensing a surge voltage;
said first circuit preventing said FET from conducting current when said first circuit is activated; and,
said second circuit resetting the flip-flop circuit after a predetermined time.

2. The circuit of 1, wherein:
said first circuit comprises clamp means for clamping the gate of said FET to ground in response to a surge to prevent charge build-up on the gate.

3. The circuit of 2, further comprising a first transistor connected to said flip-flop to saturate when the flip-flop is clocked;
a second transistor connected to the first transistor to turn on rapidly by the first trnasistor conducting; and,
a shorting pathway closed by said first and second transistors from RING lead to ground to discharge stray capacitance including the FET capacitance.

4. The circuit of 3, further comprising:
a rectifier bridge circuit connected between TIP and RING to insure positive voltage to the drain of the FET.

5. The circuit of 4, further comprising:
a resistor-capacitor series circuit connected across TIP and RING to serve as a dummy load for the RING signal.

6. The circuit of 5 further comprising:
an electronic inductor for said modem including said first and second transistors and a parallel resistor-capacitor circuit.

7. The circuit of 1, wherein:
said sensing means comprises a series circuit consisting of a capacitor and two resistors with a common point to both resistors being connected to the clock input of said JK flip-flop, the relative values of said resistors determining the point on the surge which activates the flip-flop.

8. The circuit of 1 wherein:
said first circuit comprises a clamping transistor connected to the Q bar output of the flip-flop and being connected across the source-gate of said FET to ground the gate when the flip-flop is clocked.

9. The circuit of 1, wherein:
said second circuit comprises a resistor-capacitor network connected to flip-flop output Q bar for charging the capacitor, and connected to flip-flop CLEAR for discharging when the flip-flop is clocked to maintain the gate grounding of the FET until after the surge has disappeared.

10. A modem without a conventional isolation transformer, comprising in combination:
a transformerless Data Access Arrangement in communication with the telephone line system;
an Integrated Analog device;
a Digital Signal Processor;
a Microprocessor;
the Integrated Analog device connected to the Data Access Arrangement and the Microprocessor connected to the Digital Signal Processor;
pulse transformer means connected between the Integrated Analog device and the Digital Signal Processor;
TIP and RING leads for communication between the telephone lines and the modem;
a FET connected to open and close one of said leads;
an ON/OFF HOOK circuit for supplying operating voltage to said FET when in the OFF HOOK mode;

a first circuit and a second circuit;

a flip-flop circuit for activating said first circuit in one condition and said second circuit in its other condition;

sensing means connected across said leads for activating said flip-flop circuit to said one condition upon sensing a surge voltage;

said first circuit preventing said FET from conducting current when said first circuit is activated; and,

said second circuit resetting the flip-flop circuit after a predetermined time.

11. The circuit of 10, further comprising:

multiplexer means in the Integrated Analog device for the received signal and demultiplexer means in the Digital Signal Processor for the received signal;

further multiplexer means in the Digital Signal Processor for the transmitted signal and further demultiplexer means in the Integrated Analog device for the transmitted signal, all of said signals passing through the pulse transformers being digital whereby analog distortion is avoided.

12. The circuit of 11, further comprising:

clamp means for clamping the gate of said FET to ground in response to a surge to prevent charge build-up on the gate.

13. The circuit of 12, further comprising:

a first transistor connected to said flip-flop to saturate when the flip-flop is clocked;

a second transistor connected to the first transistor to turn on rapidly by the second transistor conducting; and,

a shorting pathway closed by said first and second transistors from RING lead to ground to discharge stray capacitance including the FET capacitance.

14. The circuit of 13, further comprising:

a rectifier bridge circuit connected between TIP and RING to insure positive voltage to the drain of the FET.

15. The circuit of 14, further comprising:

a resistor-capacitor series circuit connected across TIP and RING to serve as a dummy load for the RING signal.

16. The circuit of 15 further comprising:

an electronic inductor for said modem including said first and second transistors and a parallel resistor-capacitor circuit.

17. The circuit of 10, wherein:

said sensing means comprises a series circuit comprising of a capacitor and two resistors with a common point to both resistors being connected to the clock input of said flip-flop, the relative values of said resistors determining the point on the surge which activates the flip-flop.

18. The circuit of 10 wherein:

said first circuit comprises a clamping transistor having its base connected to the Q output of the flip-flop and being connected across the source-gate of said FET to ground the gate when the flip-flop is clocked.

19. The circuit of 10, wherein:

said second circuit comprises a resistor-capacitor network connected to flip-flop output Q bar for charging the capacitor, and connected to flip-flop CLEAR for discharging when the flip-flop is clocked to maintain the gate grounding of the FET until after the surge has disappeared.

20. A surge protection circuit, comprising in combination:

a pair of input leads;

a FET connected to open and close one of said leads;

a terminal for supplying operating voltage to said FET;

a first circuit and a second circuit;

a flip-flop circuit for activating said first circuit in one condition and said second circuit in its other condition;

sensing means connected across said leads for activating said flip-flop circuit to said one condition upon sensing a surge voltage;

said first circuit preventing said FET from conducting current when said first circuit is activated; and,

said second circuit resetting the flip-flop circuit after a predetermined time.

21. A surge protection method for a device connected across a pair of incoming lines comprising the steps of:

disposing a FET in one of the incoming lines for opening and closing said line;

sensing a surge voltage;

preventing said FET from conducting current when said surge is sensed; and

maintaining the preventing until the surge has passed.

22. The method of 21, wherein:

clamping the gate of said FET to ground to prevent charge buildup on the gate in the event the surge occurs while said FET is non-conducting or conducting.

23. The method of 22, wherein:

providing a discharge path for energy passing through said FET as it is turned from ON to OFF.

24. The method of 21, wherein:

enabling a stray capacitance discharge path when said surge is sensed including the FET capacitance.

Claims

1. A modem surge protection circuit, comprising in combination:
TIP and RING leads for communication between the telephone lines and the modem;
a FET connected to open and close one of said leads;
an ON/OFF HOOK circuit for supplying operating voltage to said FET when in the OFF HOOK mode;
a modem power source for dc voltage which is positive relative to ground;
a first circuit and a second circuit;
a flip-flop circuit for activating said first circuit in one condition and said second circuit in its other condition;
sensing means connected across said leads for activating said flip-flop circuit to said one condition upon sensing a surge voltage;
said first circuit preventing said FET from conducting current when said first circuit is activated; and,
said second circuit resetting the flip-flop circuit after a predetermined time.

2. The circuit of Claim 1, wherein:
said first circuit comprises clamp means for clamping the gate of said FET to ground in response to a surge to prevent charge build-up on the gate.

3. The circuit of Claim 2, further comprising a first transistor connected to said flip-flop to saturate when the flip-flop is clocked;
a second transistor connected to the first transistor to turn on rapidly by the first trnasistor conducting; and,
a shorting pathway closed by said first and second transistors from RING lead to ground to discharge stray capacitance including the FET capacitance.

4. The circuit of Claim 3, further comprising:
a rectifier bridge circuit connected between TIP and RING to insure positive voltage to the drain of the FET.

5. The circuit of Claim 4, further comprising:
a resistor-capacitor series circuit connected across TIP and RING to serve as a dummy load for the RING signal.

6. The circuit of Claim 5 further comprising:
an electronic inductor for said modem including said first and second transistors and a parallel resistor-capacitor circuit,
wherein:
said sensing means comprises a series circuit consisting of a capacitor and two resistors with a common point to both resistors being connected to the clock input of said JK flip-flop, the relative values of said resistors determining the point on the surge which activates the flip-flop,
wherein:
said first circuit comprises a clamping transistor connected to the Q bar output of the flip-flop and being connected across the source-gate of said FET to ground the gate when the flip-flop is clocked, and
wherein:
said second circuit comprises a resistor-capacitor network connected to flip-flop output Q bar for charging the capacitor, and connected to flip-flop CLEAR for discharging when the flip-flop is clocked to maintain the gate grounding of the FET until after the surge has disappeared.

7. A modem without a conventional isolation transformer, comprising in combination:
a transformerless Data Access Arrangement in communication with the telephone line system;
an Integrated Analog device;
a Digital Signal Processor;
a Microprocessor;
the Integrated Analog device connected to the Data Access Arrangement and the Microprocessor connected to the Digital Signal Processor;
pulse transformer means connected between the Integrated Analog device and the Digital Signal Processor;
TIP and RING leads for communication between the telephone lines and the modem;
a FET connected to open and close one of said leads;
an ON/OFF HOOK circuit for supplying operating voltage to said FET when in the OFF HOOK mode;
a first circuit and a second circuit;
a flip-flop circuit for activating said first circuit in one condition and said second circuit in its other condition;
sensing means connected across said leads for activating said flip-flop circuit to said one condition upon sensing a surge voltage;
said first circuit preventing said FET from conducting current when said first circuit is activated; and,
said second circuit resetting the flip-flop circuit after a predetermined time.

8. A surge protection circuit, comprising in combination:
a pair of input leads;
a FET connected to open and close one of said leads;
a terminal for supplying operating voltage to said FET;
a first circuit and a second circuit;
a flip-flop circuit for activating said first circuit in one condition and said second circuit in its other condition;
sensing means connected across said leads for activating said flip-flop circuit to said one condition upon sensing a surge voltage;
said first circuit preventing said FET from conducting current when said first circuit is activated; and,
said second circuit resetting the flip-flop circuit after a predetermined time.

9. A surge protection method for a device connected across a pair of incoming lines comprising the steps of:
disposing a FET in one of the incoming lines for opening and closing said line;
sensing a surge voltage;
preventing said FET from conducting current when said surge is sensed; and
maintaining the preventing until the surge has passed.

10. The method of Claim 9, wherein:
clamping the gate of said FET to ground to prevent charge buildup on the gate in the event the surge occurs while said FET is non-conducting or conducting,
wherein:
providing a discharge path for energy passing through said FET as it is turned from ON to OFF, and
wherein:
enabling a stray capacitance discharge path when said surge is sensed including the FET capacitance.

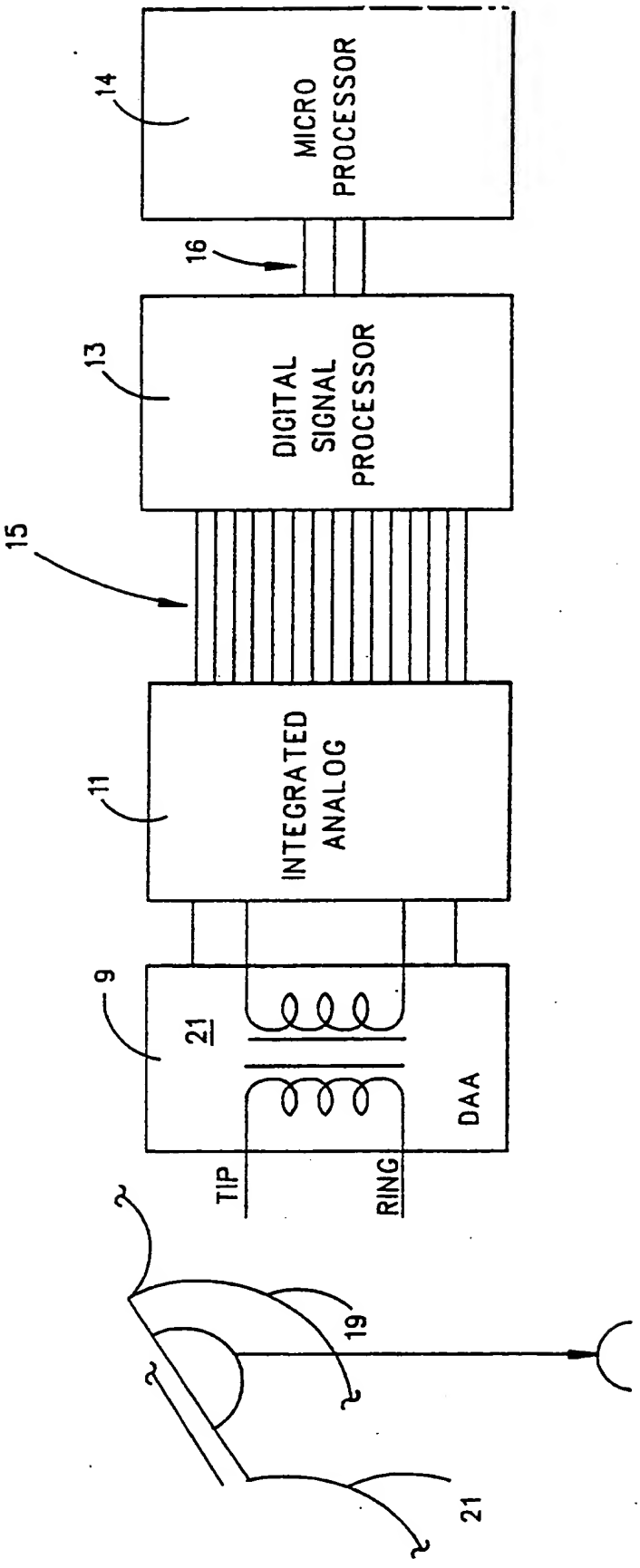


FIG. 1 PRIOR ART

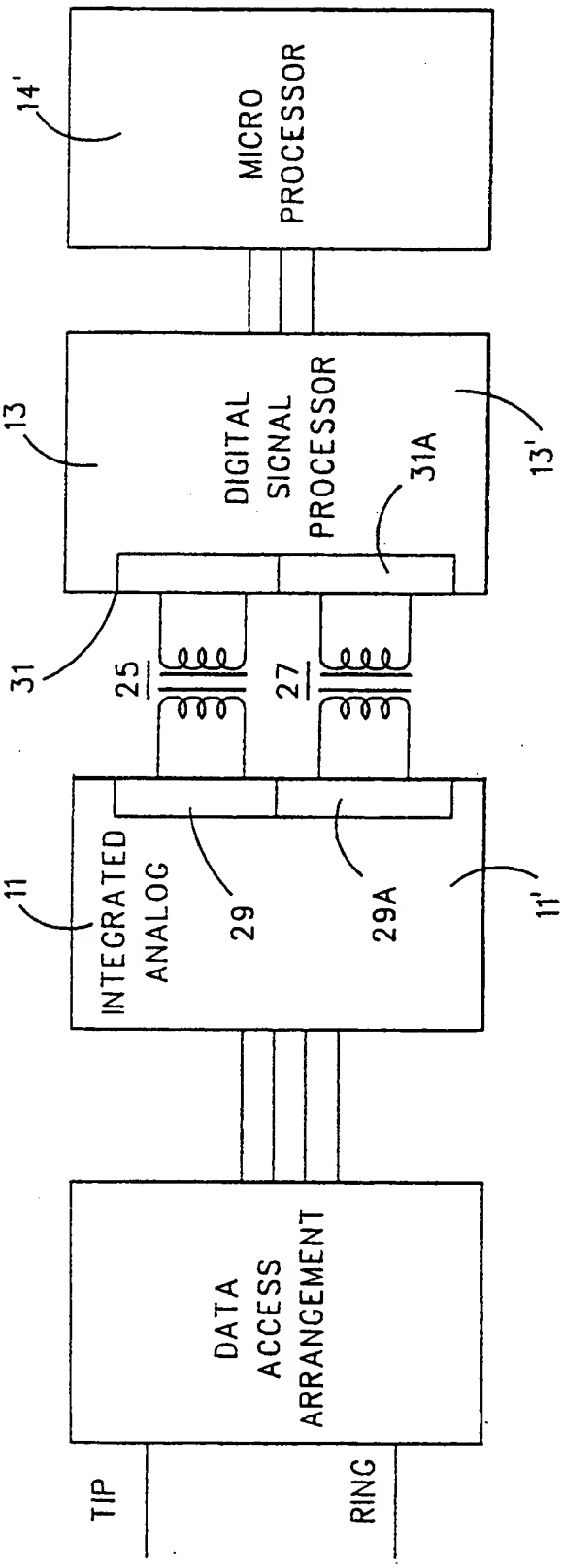

MICRO PROCESSOR
14'
DIGITAL SIGNAL PROCESSOR
13
13'
31A
31
25
27
INTEGRATED ANALOG
11
11'
29
29A
DATA ACCESS ARRANGEMENT
TIP
RING

FIG. 2

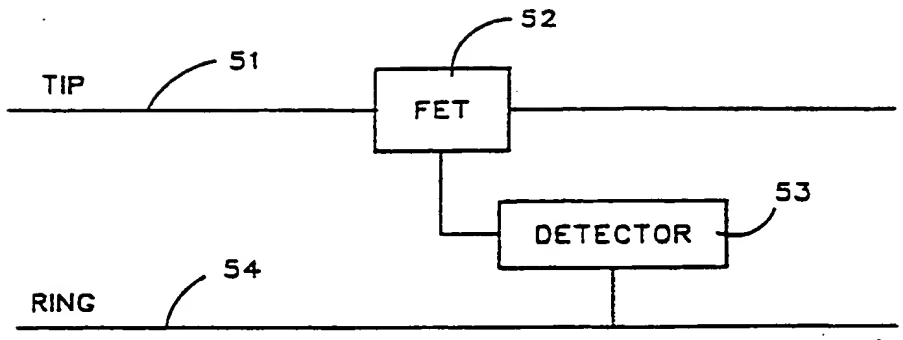


FIG. 3

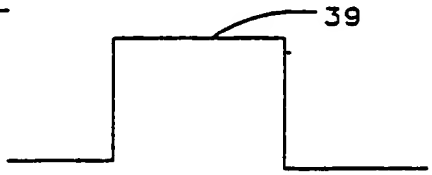


FIG. 4

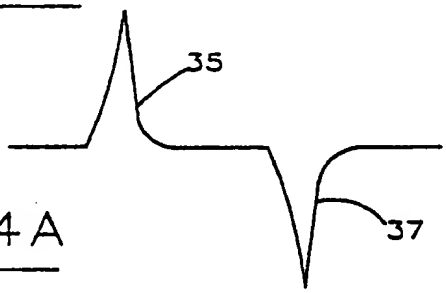


FIG. 4A

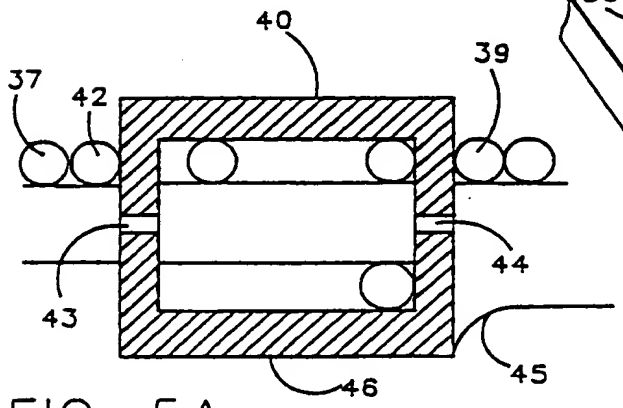


FIG. 5A

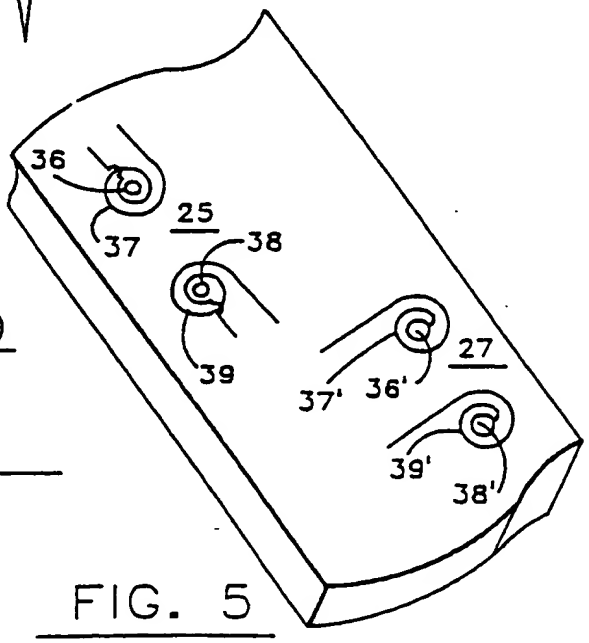


FIG. 5

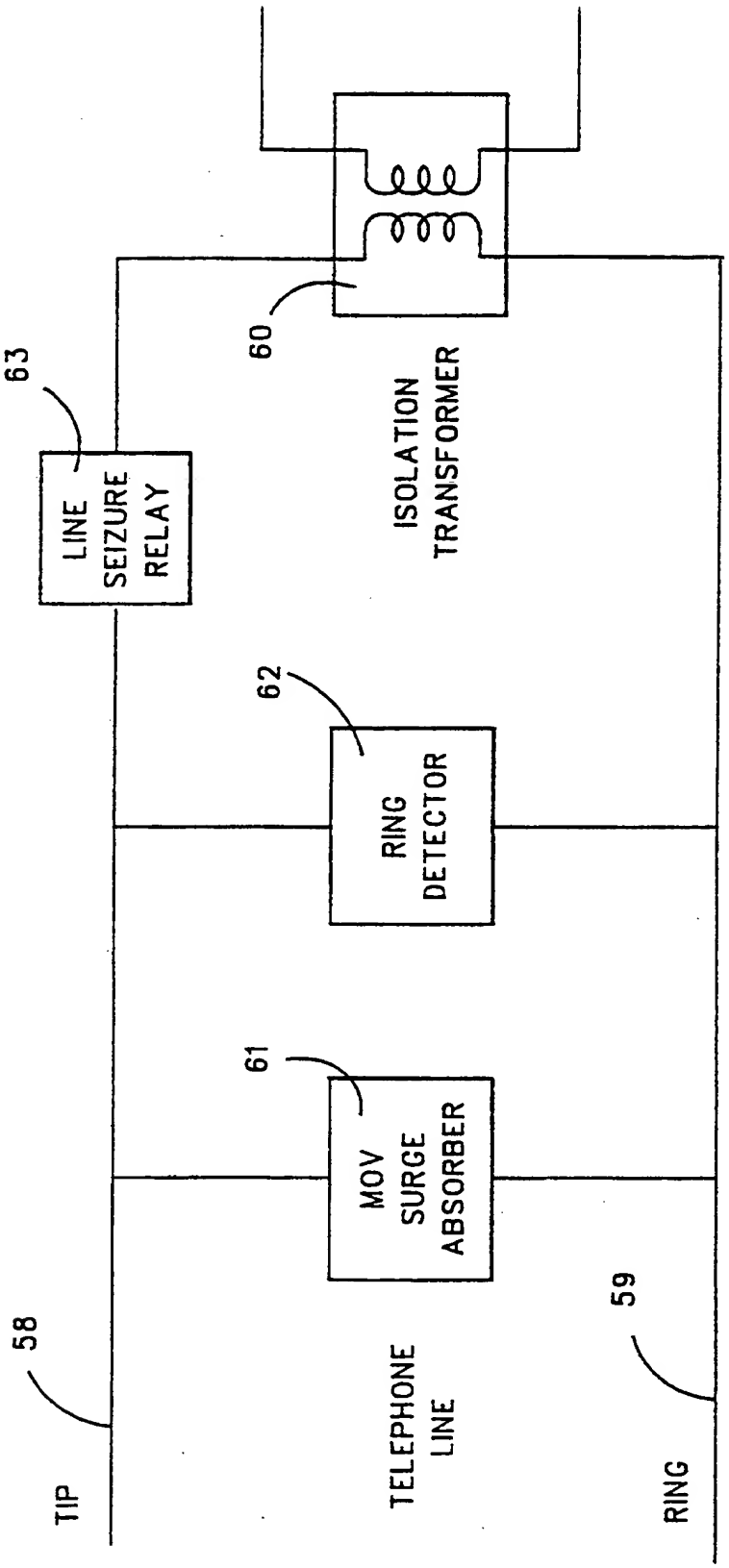


FIG. 6 PRIOR ART

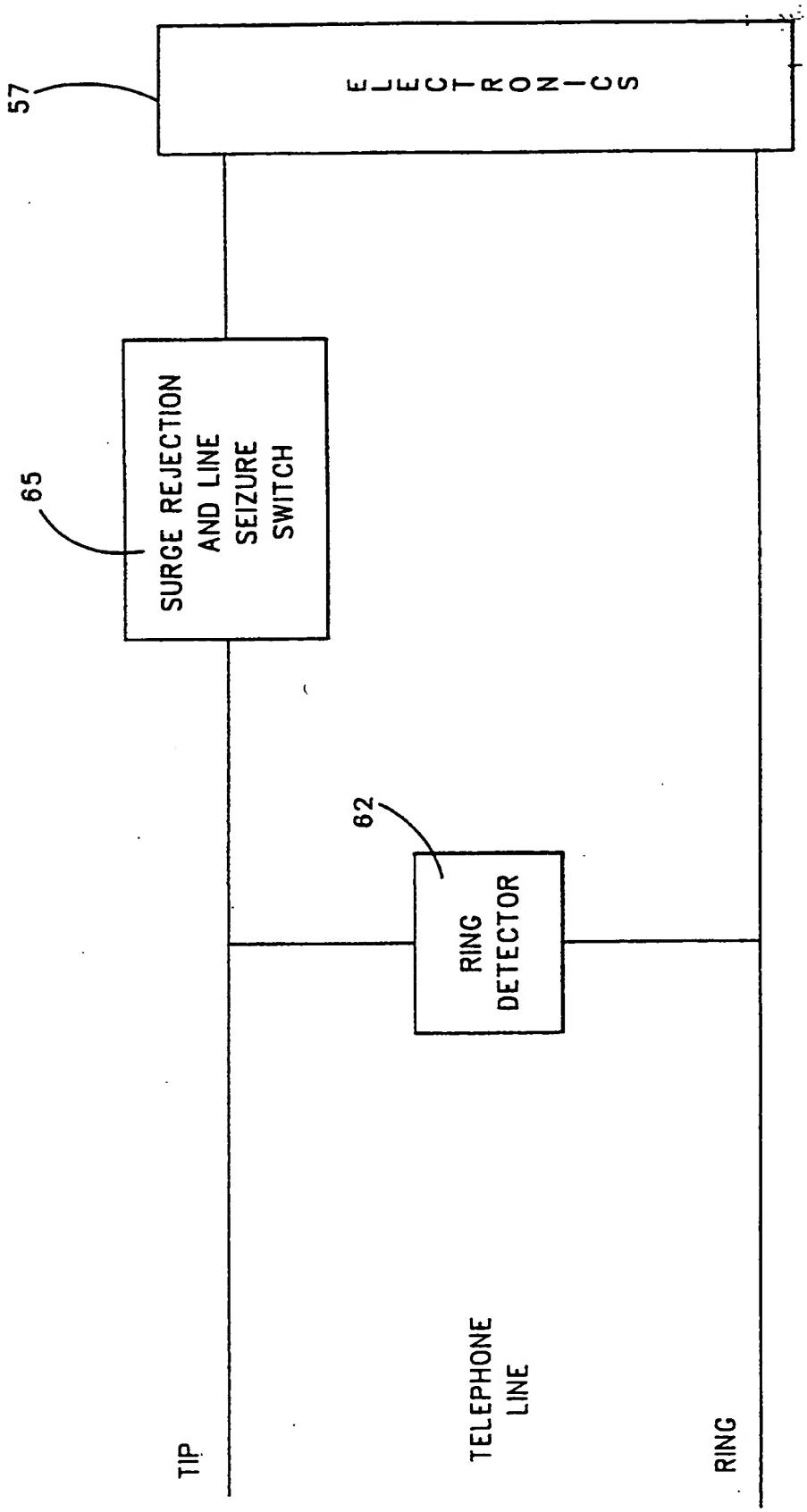
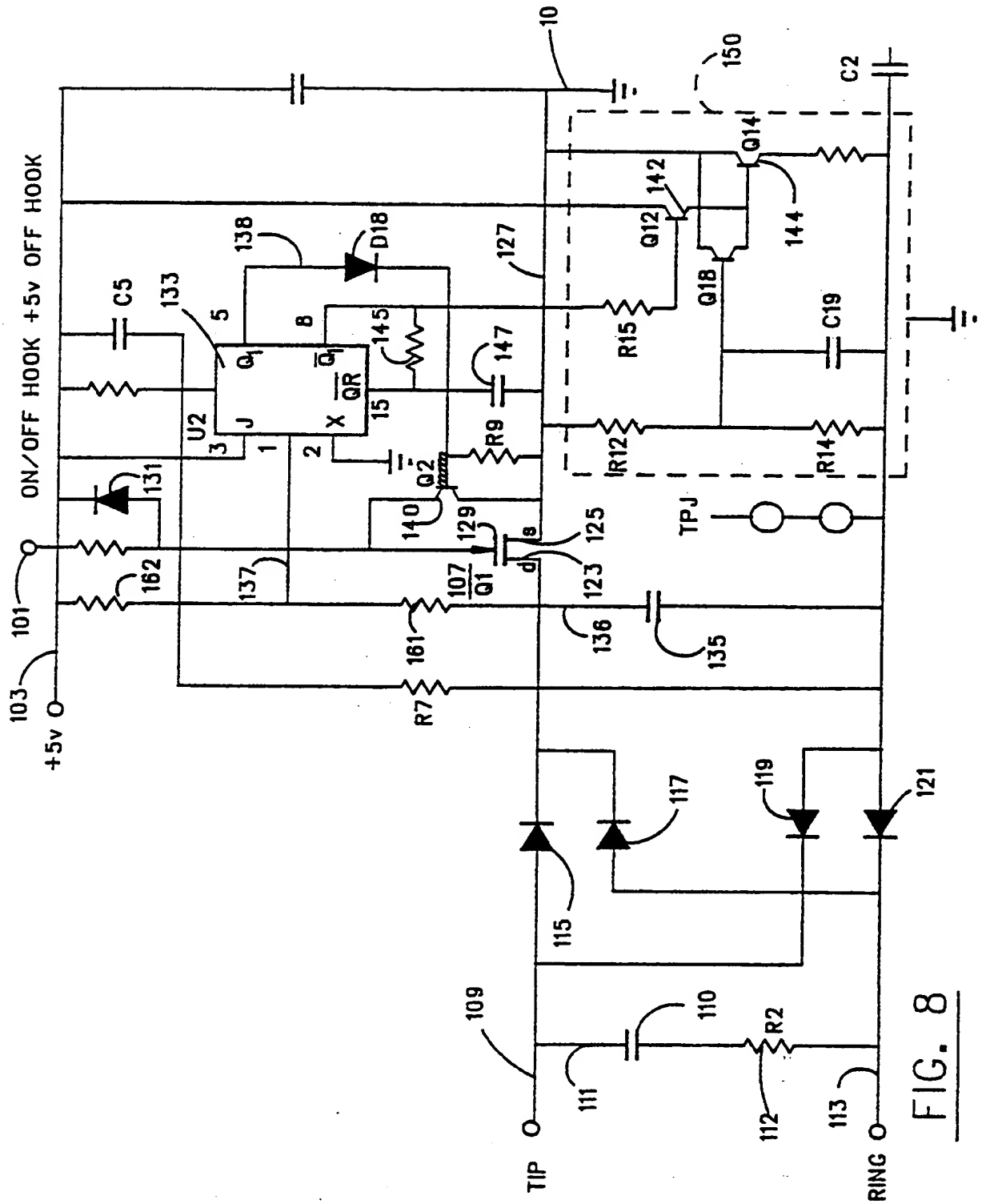

57
ELECTRONICS
65
SURGE REJECTION AND LINE SEIZURE SWITCH
62
RING DETECTOR
TIP
TELEPHONE LINE
RING

FIG. 7


ON/OFF HOOK +5v OFF HOOK
+5v
TIP
RING
TPJ
U2
Q1
Q2
Q12
Q14
Q18
D18
R2
R7
R9
R12
R14
R15
C2
C5
C19
10
101
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107
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FIG. 8

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(54) Active surge rejection circuit.

(57) The ACTIVE SURGE REJECTION CIRCUIT uses a FET connected in one of the TIP and RING leads to open and close the lead. A JK flip-flop is connected to a voltage sensing circuit which senses voltage surges and clocks the flip-flop early in the voltage rise. This activates a first circuit to ground the FET gate and hold the FET open. Meanwhile, a second circuit comprising an RC circuit charges a capacitor which maintains the FET in its OFF condition for a period of time longer than the surge, i.e., about 1 m sec, and then clears the JK flip-flop after the capacitor has discharged a predetermined amount.

The combination of this invention and a transformerless DAA with pulse transformer digital isolation at the digital interface between the IA and the DSP synergistically provides both common and uncommon mode protection.

EP 0 576 883 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 93109224.1

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US - A - 4 979 071 (TAKAAKI ITO) * Totality * --	1,8, 9,10	H 02 H 3/22 H 02 H 3/00 H 02 H 9/04 H 04 M 11/00
A	US - A - 4 647 721 (V.A. BUSAM) * Abstract; claims; fig. 1,2 * --	1,8, 9,10	H 04 M 19/00
A	US - A - 4 465 903 (A.C. BARBER) * Abstract; column 1, line 61 - column 3, line 3; claims; fig. 1,2,3 * --	1,8, 9,10	
A	US - A - 4 433 212 (D.W. MOSES) * Abstract; column 2, lines 17-64; column 3, lines 9-30; claims; fig. 1,2 * --	1	
A	US - A - 4 398 066 (H. SINBERG) * Totality * --	1,8, 9,10	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 02 H 3/00 H 02 H 7/00 H 02 H 9/00 H 04 M 9/00 H 04 M 11/00 H 04 M 19/00
A	US - A - 4 203 006 (R.C. MASCIA) * Abstract; column 2, lines 8-37; claims; fig. 1,2,3 * --	1,8, 9,10	
A	US - A - 4 079 211 (D.J.G. JANSSSEN) * Totality * --	1,8, 9,10	
A	FR - A - 2 495 866 (TELECOMMUNICATIONS) * Claims; fig. 1,2,3 * ----	1,8, 9,10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	31-08-1994	ERBER

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